(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 250 078 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 87303971.3

(51) Int. Cl.4: H01L 23/52

(22) Date of filing: 01.05.87

A request for correction of the description has been filed pursuant to Rule 88 EPC. A decision on the request will be taken during the proceedings before the Examining Division (Guidelines for Examination in the EPO, A-V, 2.2).

(30) Priority: 09.05.86 US 861519

(43) Date of publication of application:
23.12.87 Bulletin 87/52

(84) Designated Contracting States:
AT BE CH DE ES FR GB GR IT LI LU NL SE

(71) Applicant: ACTEL CORPORATION
320 Soquel Way
Sunnyvale California 94086(US)

(72) Inventor: Mohsen, Amr M.
4076 Sobey Court
Saratoga California 95070(US)
Inventor: McCollum, John L.
19810 Merribrook Drive
Saratoga California 95070(US)
Inventor: Hamdy, Esmat Z.
4486 Ariel
Fremont California 94536(US)

(74) Representative: Williams, Trevor John et al
J.A. KEMP & CO. 14 South Square Gray's Inn
London WC1R 5EU(GB)

(54) Programmable low-impedance interconnect circuit element and method of forming thereof.

(57) A programmable interconnect device for use in integrated circuits comprises a first conductive layer, an insulating layer over said first conductive layer, and a second conductive layer over said insulating layer. There is described the application of a programming voltage to cause the formation of at least one controlled radius filament formed from at least one of said first or second conductive layers, this may have a resistance of less than 300 Ohms. Suitably, the first conductive layer may be a polysilicon and the insulating layer a silicon nitride. The invention also relates to the method of forming such a circuit element on a substrate in a CMOS or bipolar application process.

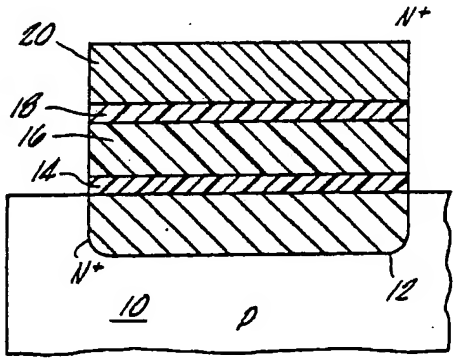

FIG. 1.

EP 0 250 078 A2

manufacture with standard semiconductor processing. Capacitors with silicon oxides used as a dielectric do not produce a low enough impedance after programming.

Examples of known anti-fuse elements are found in the prior art. Reference is made to: U.S. Patent No. 3,423,646 which uses aluminum oxide, cadmium sulfide; U.S. Patent No. 3,634,929 which uses single film of AL_2O_3, SiO_2, and Si_3N_4; U.S. Patent No. 4,322,822 which uses SiO_2; U.S. Patent No. 4,488,262 which uses oxide or titanate of a transition metal; U.S. Patent No. 4,499,557 which uses doped amorphous silicon alloy; U.S. Patent No. 4,502,208 which uses SiO_2; U.S. Patent No. 4,507,757 which uses SiO_2; U.S. Patent No. 4,543,594 which uses SiO_2.

Most of THe above patents either describe complicated technologies or need high breakdown voltages and currents, and or are difficult to manufacture or do not meet the reliability requirements of state-of-the-art integrated circuits in both the on and off states. These patents do not disclose the creation of controllable conductive filaments with low resistance after programming.

Other problems associated with existing dielectric materials in anti-fuse links include large memory cells, complex manufacturing processes of the unblown anti-fuse elements.

OBJECTS AND ADVANTAGES

An object of the present invention is to provide an electrically programmable low-impedance interconnect element.

Another object of the present invention is to provide an electrically programmable interconnect element which may be programmed with sufficiently low voltages and currents compatible with state-of-the-art MOS technology, resulting in a low impedance in the on-state.

Another object of the present invention is to provide an electrically-programmable interconnect element which is manufacturable using standard semiconductor processing and has high reliability in both the on and off states.

Advantages associated with the present invention in some or all of its embodiments include an interconnect which can be made with standard semiconductor manufacturing techniques, small size, a high reading current after programming, a manufacturing process with a minimal number of steps, and a controlled radius interconnect filament through the dielectric resulting in a repeatably manufacturable controlled low resistance link after programming. Furthermore, the present invention is characterized by high reliability in both the programmed and unprogrammed state. Other and further advantages of the present invention will appear hereinafter.

SUMMARY OF THE INVENTION

An electrically Programmable, Low-Impedance Circuit Element after programming ("PLICE") is described. It consists of a capacitor-like structure with very low leakage current before programming and a low-resistance after programming.

This PLICE element is formed by having a dielectric between two conductive electrodes. In a preferred embodiment, one or both of the two conductive electrodes may be made of a high electromigration immunity material and may be formed from either heavily doped polysilicon, heavily doped single crystal silicon, or refractory metal such as tungsten, molybdenum, platinum, titanium, tantalum, or their silicides or a sandwich of polysilicon and metal. Those of ordinary skill in the art will recognize that the metal may be any substance used to provide interconnect in integrated circuits or is used as a diffusion barrier. In addition, it is believed that combinations of the above material will function in the present invention. In other embodiments, lower electromigration immunity materials may be used as long as the current passed through the PLICE after programming is appropriately limited to assure proper lifetime.

The dielectric layer, single or composite, between the two electrodes is such that when it is disrupted by a high electric field it will facilitate the flow of one of the two electrodes to produce a controlled radius conductive filament during its breakdown. It requires a low amount of charge fluence to breakdown at the higher programming voltage with practically used voltages and currents in integrated circuits. It also has a large enough charge fluence to breakdown at normal operating voltages to be a reliable circuit element during operation in its off state.

During programming, as the applied voltage reaches the dielectric breakdown, a localized weak spot in the dielectric starts to carry most of the leaking current and heats up which, in turn, increases the leakage current. A thermal runaway condition develops which results in localized heating and melting of the dielectric and adjacent electrode material. The conductive material flows from one of the two electrodes and forms a conductive filament shorting both electrodes. The thickness of this electrode should be sufficient not to cause any discontinuity or pits during the filament formation. The final radius of the filament depends on the composition and thickness of the dielectric, the

ing a sheet resistance of approximately 10 to 100 ohms/square. The thickness of the polysilicon may be from approximately 500 to 10,000 Angstroms, and may be approximately 4500 Angstroms in a preferred embodiment.

The top electrode 20 may also be a sandwich of said polysilicon layer and on top of it a conductive metal layer of Aluminum approximately 5,000 to 15,000 Angstroms.

In this embodiment, the thickness of the bottom oxide layer 14 of the composite dielectric is from 20 to 50 Angstroms, the thickness of the central silicon nitride layer is from 40 to 100 Angstroms, and the thickness of the top oxide layer 18 is from 0 to 50 Angstroms. The relative thickness of these layers are essential for manufacturing a reliable PLICE and a controlled filament of specific radius and conductivity as will be disclosed further herein.

The PLICE element of this embodiment is programmed by applying a current-controlled voltage source across the two electrodes. The composition of the composite dielectric is such that the structure provides an on-resistance of less than 300 ohms after programming and an off-resistance of more than 100 mega ohms before programming. The structure requires a programming pulse of magnitude less than 30 volts, a time duration of less than 100 mSec at a current of less than 10 mAmps. The size of the conductive filament is a function of the programming pulse and of the composition of the composite dielectric structure and its effective radius is in the range of from .02 uM to 0.2 um.

As an example, a PLICE element having an N-diffusion of $1x10^{21}$ atoms/cm lower electrode, a 4500 Angstrom highly-doped polysilicon upper electrode having a sheet resistance of 18 ohms/square, and a dielectric consisting of a first layer of approximately 40 Angstroms of Silicon dioxide (SiO_2), a second layer of approximately 70 Angstroms of silicon nitride (Si_3N_4), and a third layer of approximately 15 Angstroms of SiO_2 will produce a filament having an effective radius of approximately 0.05 microns if programmed with a pulse of approximately 18v and a current of 1.0 mA for 100 mSec of duration. It has been found that the resulting filament resistance is less than 40 ohms. For the same 18V programming voltage and 100 mSec of programming time a current of 0.2mA and 10mA will produce a filament with effective radius from 0.04 microns to 0.2 microns

It will be appreciated by those skilled in the art that conductivity of the dopants of substrate 10 lower electrode 12 and upper electrode 20 may be reversed i.e. substrate 10 may be N-type material and lower and upper electrodes 12 and 20 may be heavily doped P material.

Referring now to FIGS. 2a and 2b, an alternate embodiments of the PLICE will be disclosed wherein the two electrodes are above the substrate. These embodiments facilitate the interconnect between two conductors without using the silicon substrate as a path. Hence, the substrate can be used for active devices.

Referring first to FIG. 2a the bottom electrode 40 of the PLICE element is fabricated of polysilicon which may be from approximately 500 to 10,000 Angstroms thick covered by a silicide layer 42, which may be from approximately 100 to 5000 Angstroms thick. This reduces the sheet resistance of the polysilicon to less than approximately 10 ohms. Silicide layer 42 also serves to provide the molten substance which will create the filament through the dielectric. Silicide layer 42 may be of a silicide of tungsten, molybdenum, titanium or tantalum. Insulating oxide regions 44 are shown in FIG. 2a to indicate the type of environment which may be typically provided to isolate the PLICE element from other circuit elements on the silicon substrate.

Dielectric layer 46 is placed over the silicide layer 42 and also overlaps field oxide region 44. Dielectric layer 46 of the embodiment of FIG. 2a may be the sandwich structure disclosed with respect to the embodiment of FIG. 1. Dielectric layer 46 may also be formed of a single silicon nitride layer approximately 100-2000 Angstroms thick.

A barrier metal layer 48, such as titanium, tungsten, or titanium nitride is placed in between dielectric 46 and top electrode 50 (which may be made of aluminum) to prevent the diffusion of the material of the top electrode into the filament that is formed after programming. Barrier metal layer 48 may be from approximately 50 to 5000 Angstroms thick.

Turning now to FIG. 2b the PLICE element of this embodiment has a lower electrode 60 which may be a metal such as aluminum, covered with a layer of barrier metal, such as tungsten, titanium, or titanium nitride to prevent the diffusion of the aluminum metal into the filament as discussed with respect to FIG. 2a. Insulating oxide regions 64 are shown as a method to isolate the PLICE element from other circuit elements on the silicon substrate. A layer 66, preferably formed of tungsten silicide is interposed between barrier metal layer 62 and dielectric layer 68 through which the filament will be formed. Layer 66 is used to provide the molten substance from which the filament will be formed when the PLICE element is programmed. A barrier metal layer 70 is interposed between dielectric layer 68 and top electrode 72, which may be a

next deposited using standard LPCVD or CVD techniques. A final layer of silicon dioxide is then either deposited or thermally grown. The processes used to form these layers may be conventional processing steps known to those skilled in the art.

Referring now to FIG. 6c, a layer polycrystalline silicon region 172 is then formed over the entire surface of the wafer. Region 172 may be fabricated with standard LPCVD or CVD techniques. Referring to FIG. 6c, a photomask 174 has been used to delineate the polycrystalline silicon layer 172 to form the upper electrode of the PLICE. This shaped upper electrode 176 is then used as a mask to selectively remove the silicon dioxide/silicon nitride/silicon dioxide dielectric sandwich insulating layer from areas outside of the PLICE structure. The structure is then sealed with a thin thermal oxide layer 178, as shown in FIG. 6d.

The process of manufacturing the remainder of the CMOS circuit can then continue in a standard manner to form the finished device as illustrated in FIG. 6a. The boron source and drain regions 180 and 182 for the P-channel devices are implanted, using a photomask 184 and the portion of polysilicon gate layer 162 to protect the areas outside the implant regions. Referring to FIG. 6f, a polysilicon glass passivation layer 186 is deposited, flowed and contact cuts are made. Metal layer 188 is then deposited and delineated making connections to the transistors PLICE nodes. If dual layer metal is to be used, an interlayer dielectric is deposited and a second layer of metal is deposited, delineated and annealed (not shown). Finally, a passivation layer is deposited for scratch protection and the metal pads are opened.

The PLICE element can also be applied to bipolar process for either PROM cells or programmable logic devices. The preferred embodiment would be the same as the Cmos embodiment. Such a process is disclosed in conjunction with FIG. 7. The process would begin as a conventional bipolar process, first the buried layer would be defined and diffused in, followed by the epitaxial deposition and isolation process. There are several methods for performing isolation and diffusion, all of which will work with the PLICE element. The base region would then be defined and diffused. The emitter would then be defined and diffused followed by the contact cuts. This is the preferred point where the PLICE element could be defined by forming the dielectric, followed by the poly deposition, doping and delineation. The underlying dielectric would then be removed from the unwanted areas utilizing the poly as mask. Following the definition of the PLICE element the metalization process would proceed as normal. Either single or dual metal processes may be used.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

Claims

1. A programmable low impedance interconnect circuit element, including:
a first conductive layer;
an insulating layer over said first conductive layer, and
a second conductive layer over said insulating layer, wherein the application of a programming voltage causes the formation of at least one controlled radius filament formed from at least one of the said first or second conductive layers having a resistance of less than 300 ohms.

2. A programmable low impedance interconnect circuit element, including:
a first conductive layer;
an insulating layer over said first conductive layer, said insulating layer having a first silicon dioxide portion and a second silicon nitride portion over said first silicon dioxide portion, and
a second conductive layer over said insulating layer.

3. The programmable low impedance interconnect circuit element of claim 2 wherein said insulating layer further includes a third silicon dioxide portion over said second silicon nitride portion.

4. The programmable low impedance interconnect circuit of claim 2 or 3 wherein said insulating layer contains at least one controlled-radius filament of conductive material formed from at least one of said first or second conductive layers extending therethrough and in electrical contact with said first and second conductive layers.

5. The programmable low impedance interconnect circuit of claim 1, 2, 3 or 4, wherein at least one of said conductive layers is formed of a material having a high electromigration immunity.

6. The programmable low impedance interconnect circuit of claim 1, 2, 3, 4 or 5, wherein at least one of said conductive layers is heavily doped polysilicon.

7. The programmable low impedance interconnect circuit of claim 1, 2 or 3, wherein said first conductive layer is a diffusion and wherein said second conductive layer is heavily doped polysilicon having the same polarity as said diffusion.

8. The programmable low impedance interconnect circuit of claim 7, wherein said second conductive layer is covered by a metal layer.

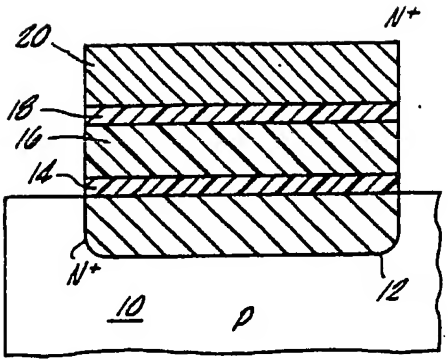

FIG. 1

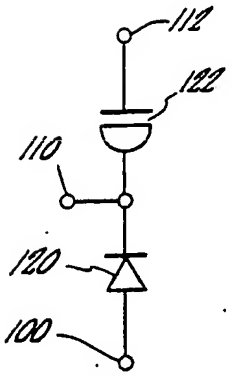

FIG. 5A

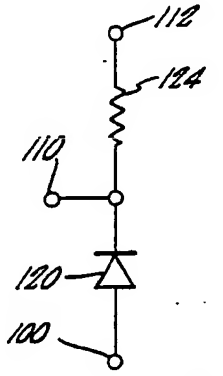

FIG. 5B

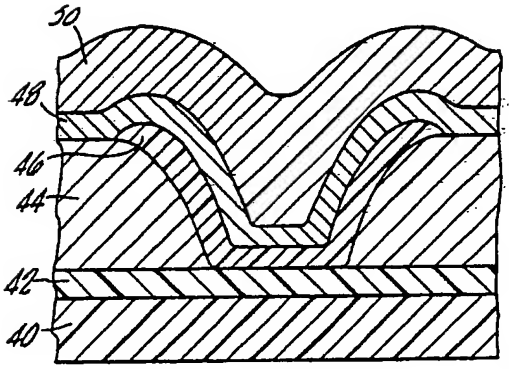

FIG. 2A

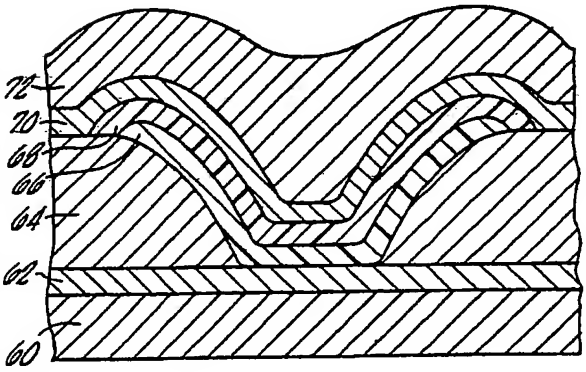

FIG. 2B

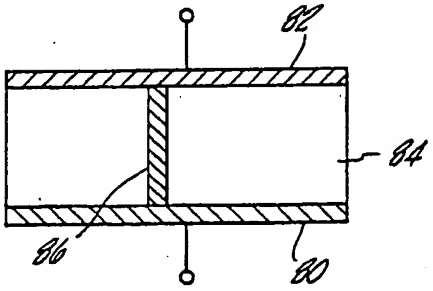

FIG. 3

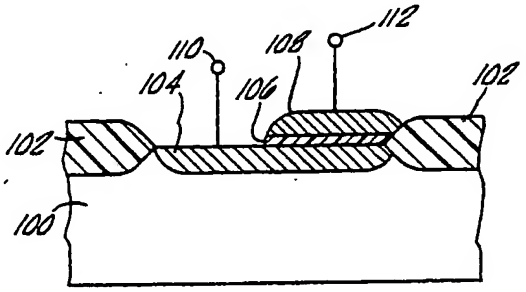

FIG. 4

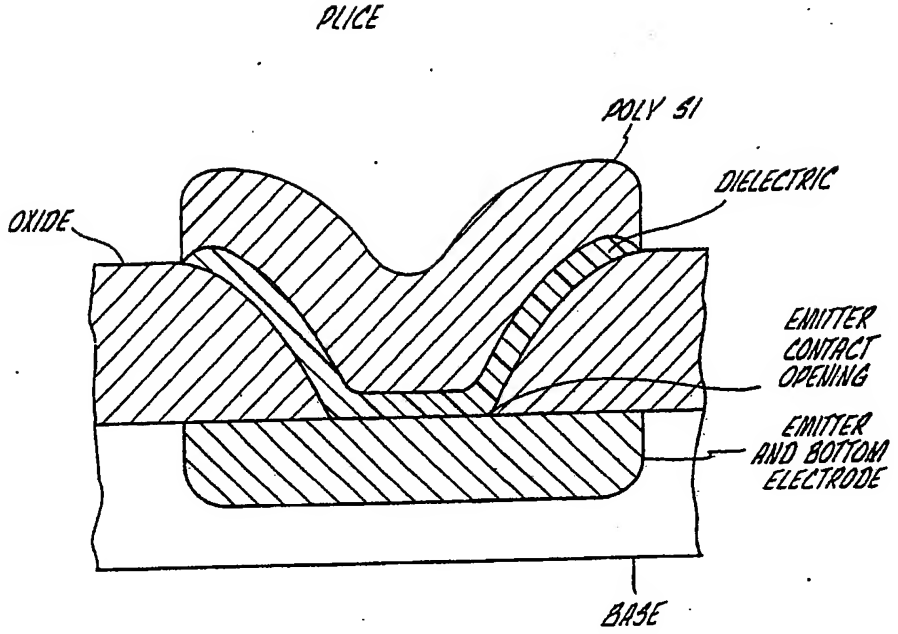

FIG. 7